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Radiation Hardening of CMOS Microelectronics

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RADIATION HARDENING OF CMOS MICROELECTRONICS

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ABSTRACT

A unique methodology, silicon transfer to arbitrary substrates, has been developed under this program and is being investigated as a technique for significantly increasing the radiation insensitivity of limited quantities of *conventional* silicon microelectronic circuits. In this approach, removal of the that part of the silicon substrate not required for circuit operation is carried out, following completion of the circuit fabrication process. This post-processing technique is therefore applicable to *state-of-the-art* ICs, effectively bypassing the 3-generation technology/performance gap presently separating today's electronics from available radiation-hard electronics. Also, of prime concern are the cost savings that result by eliminating the requirement for costly redesign of commercial circuits for Rad-hard applications. Successful deployment of this technology will result in a major impact on the radiation hard electronics community in circuit functionality, design and software availability and fabrication costs.

Introduction

The use of commercial devices in space and nuclear weapons presents unique challenges due to the potential of encountering radiation intense environments. While the total dose response of commercial devices may be improved by using shielding, shielding is not usually an effective means of improving the single event upset (SEU) response. In fact, terrestrial SEU is becoming a problem as technologies scale down, making them more sensitive to SEU. While design changes (*i.e*., adding feedback resistors, extra transistors, *etc*.) have been used to improve the SEU response of CMOS devices, these design modifications can significantly degrade the performance and manufacturability of the ICs. Thus, most commercial manufacturers will not use these techniques to improve the IC SEU response. In this work we evaluate the effectiveness and feasibility of thinning the CMOS wafer substrate of fully fabricated ICs for reducing SEU sensitivity by significantly reducing charge collection volume using our wafer thinning process.

Wafer Thinning Procedure

LLNL's standard thinning procedure was originally developed using low doped prime 4" non-epitaxial material using a wet chemical process. Unfortunately, the wet etch solution is sensitive to wafer doping concentration and type. Low doped, 10^{15} - 10^{16}/cm^2, p-type wafers maintain initial surface roughness throughout the etch, while n-type wafers showing an "orange peel" effect with average surface roughness of about 4 µm peak-to-peak. In addition, as the doping concentration is increased the effectiveness of the hydroxide-based etching to thin the material decreases. Thus, the original thinning procedures are not compatible with the 6" epitaxial wafers from Sandia's 0.5-µm non-hardened technology since the substrate doping concentration is ~10^{19}/cm^3. As such, we are in the process of modifying the thinning procedure to be compatible with epitaxial wafers and to improve uniformity of the final thin silicon layer.

The best approach to thinning epitaxial, such as used in Sandia's CMOS process, is the use of a grinding step to remove the bulk of the silicon substrate. This is followed by a high-low doping, selective wet chemical etch to remove the heavily p-type doped substrate from the low doped epitaxial material. The selective etch solution giving the best results is 1:3:8 HF(49%): HNO3(30%): CH3COOH(100%) (in volume). In this solution, the etch rate of silicon doped with boron concentration greater than 7x10^{18}/cm^3 is 2 µm/min. The rate decreases to ~0.02 µm/min at concentrations of 3x10^{17}/cm^3. While this is a new approach for the LLNL transfer process, we are confident this procedure will work.

For future work, the bonding process should be changed to render the LLNL procedure compatible with standard silicon fabrication techniques. This will be achieved by using a combination of Chemical Mechanical Planarization (CMP) and low-temperature wafer bonding. Once the new bonding procedure is established, Sandia will be capable of performing this process in house.

Detailed Thinning Procedure

Substrate thinning is accomplished by first bonding the fully processed silicon wafer circuit-side down to a support substrate. The wafer is separated from the support substrate using shims or spacers while epoxy is introduced at the edge. The epoxy wicks in by capillary action to reliable fill the 1-mil void between the two substrates. Two additional steps which can be taken to improve this step are to heat the assembled pair to

50-70ºC to lower the effective epoxy viscosity and to expedite gap filling, and to provide a constant thickness variation across the gap by filling it with glass fiber spacers of a constant dimension. Masterbond epoxy product number EP112 is employed due to its excellent resistance to the chemical solutions commonly used in silicon processing, its high optical clarity, its high shore hardness value of 93, and low viscosity of less than 200cps. A thermoset cycle of 110ºC for 2 hours, followed by 150ºC for 3 hours is employed to achieve a bonded pair. Corning 1737 glass shaped in the form of a silicon wafer and 1.1mm thick is selected as the holding substrate. This glass type is commonly employed in the manufacture of flat-panel displays due its good surface quality and optical clarity.

Once the bonding process has been completed, the silicon substrate can be thinned using the standard LLNL process. The bonded pair is inserted in a heated beaker of 3:1 H_2O:KOH at 65ºC and the etch is stopped at about 5-10µm of silicon thickness using an optical end-point detection system. Light transmitted through the thinned silicon wafer/glass bonded pair is used for the etch stopping technique – a bright red indicates a remaining silicon thickness of about 15µm. Using this wet chemical etch provides the simplest and least expensive option for bulk thinning. An example of this technique is shown in Fig. 1.

An important feature of the transfer process is maintaining the backside surface quality of the silicon wafer before and after the silicon thinning in preparation for the final patterning step. Optimal results achieve 100nm peak-to-peak average wafer backside surface roughness to satisfy the expected application requirements. As mentioned above, the etching solution is sensitive to wafer doping concentration and type. Low doped, 10^{15} - $10^{16}/cm^2$, p-type wafers maintain initial surface roughness throughout etching, with n-type wafers showing an “orange peel” effect with average surface roughness of about 4µm peak-to-peak. Low surface roughness may be achieved by preparatory treatment of the silicon surface prior to KOH bulk thinning.

Preparatory treatments may be performed using a mix-and-match of several techniques including lapping and polishing, electrochemical etching, SEZ polishing, and HF/Nitric polishing. Lapping and polishing may be used to thin the wafer and provide a satisfactory surface finish, but maintaining the TTV using this technique is inordinately expensive for most applications. Silicon spray etching equipment may also be employed to surface treat the wafer. SEZ (America) spinning and etching equipment formulates one HF:HNO_3 solution for silicon removal at an average rate of 63µm/min and a second HF:HNO_3 formulation for silicon polishing. Moderate success has been obtained with this equipment.

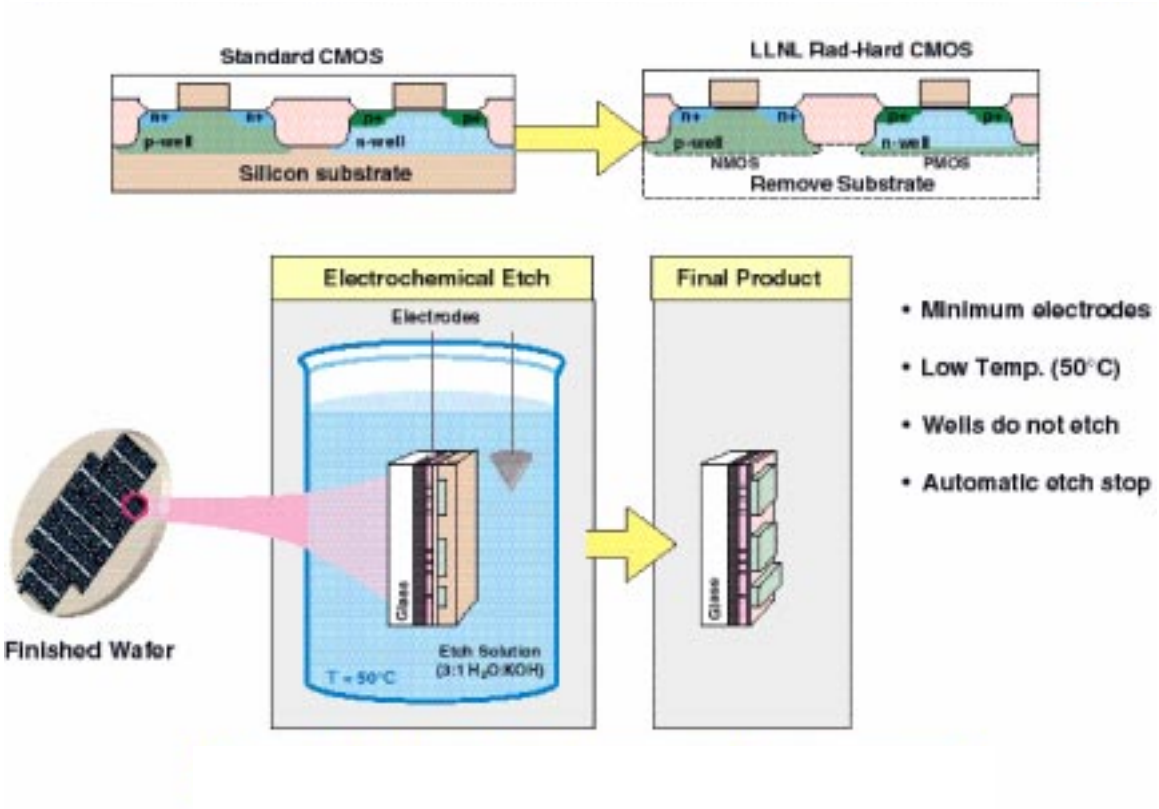

Figure 1 Example of the LLNL wafer thinning procedure.

We have successfully transferred both individual n-MOS transistors and arrays of n-MOS transistors using this technique. In Fig. 2 we show photographs and I-V characteristics from a transferred substrate. As can be seen from the I-V characteristics no degradation in electrical performance was observed.

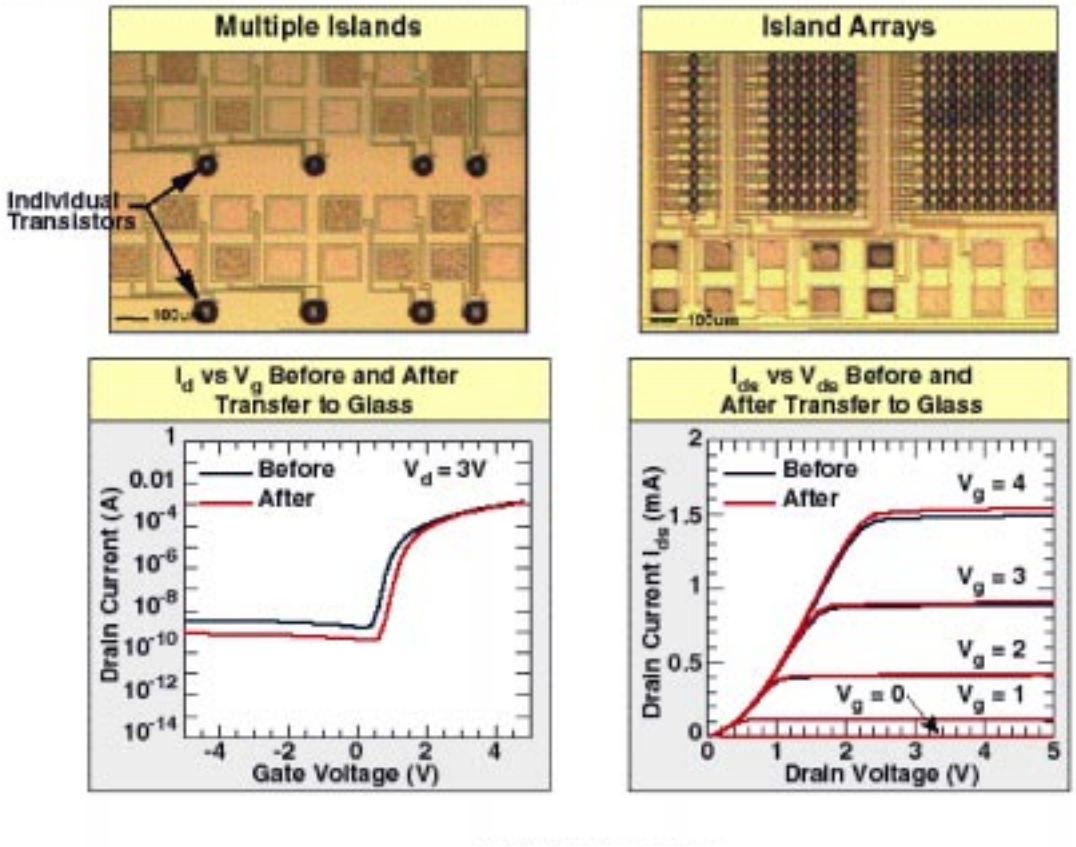

Figure 2 Example n-MOS transistors and arrays transferred using the LLNL technique. The electrical characteristics of the transistors are shownbefore and after transfer.

Simulation Results

In conjunction with Sandia we have performed three-dimensional mixed-level simulations to determine the effect of substrate thickness on the single-event upset (SEU) response of Sandia's CMOS6 16K SRAM cells. CMOS6 is a 5-V unhardened commercial technology with LOCOS isolation and an as-drawn gate length of 0.6 μm. The objective of the simulations was to determine how thin the substrate would need to be to significantly increase the SEU threshold, and to determine if substrate thinning would affect the baseline current-voltage (I-V) characteristics of the transistors.

Figure 3 shows simulated gate subthreshold I-V characteristics of a 2.3x0.6 μm n-channel CMOS6 transistor, before and after thinning to a substrate thickness of 0.5 μm. The I-V characteristics remain nominally unchanged, indicating that substrate thinning does not affect device threshold voltage. Note that for these simulations the body potential was tied using a top-side contact adjacent to the channel. This contact serves as an efficient body tie, similar to a body tie in an SOI device. Without an efficient body contact, we would expect floating body effects like those seen in SOI devices would eventually surface, because the thinned substrate transistor becomes analogous to an SOI transistor as it is thinned. The results of the simulations agree with experimental results shown in Figure 4. In Fig. 4, I-V characteristics measured before and after the wafer thinning process for transistors fabricated on four-inch diameter silicon wafers using a 2μm NMOS process are shown. Consistent with the simulations, we observe no significant

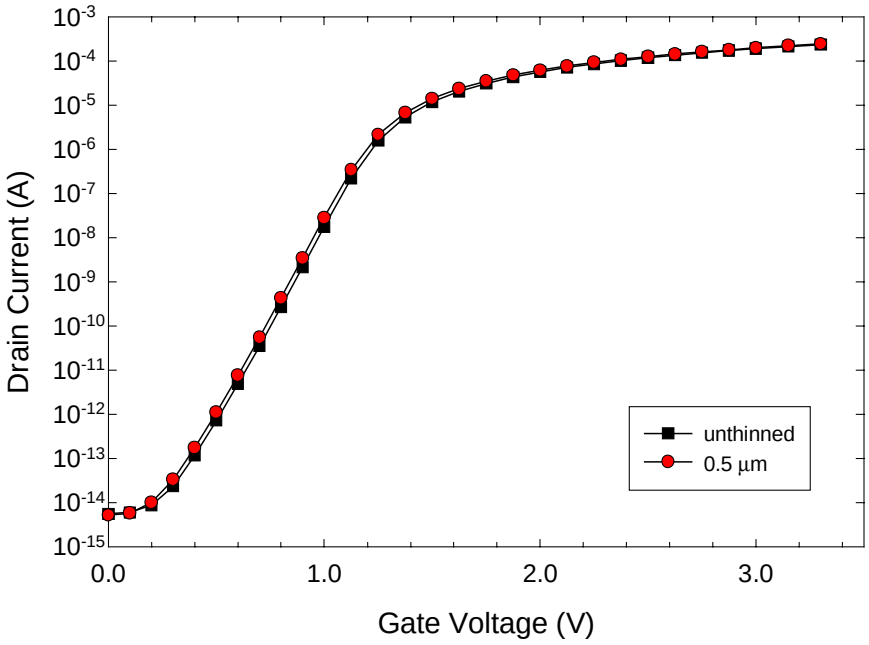

Figure 3. Simulated subthreshold current-voltage characteristics for CMOS6 2.3x0.6 μm n-channel transistors before and after thinning to a substrate thickness of 0.5 μm.

difference in the I-V characteristic before and after the wafers are thinned.

The predicted SEU response of CMOS6 transistors as they are thinned is plotted in Figure 5. This figure shows the SEU threshold on the y-axis plotted against the substrate thickness. Thresholds for two strike locations are shown: strikes to the center of the drain, and strikes to the center of the gate. The drain center is typically the most sensitive strike location for CMOS SRAMs, but in SOI devices gate strikes become important because floating body effects can trigger a parasitic bipolar transistor mechanism that limits SEU hardness. As shown in Fig. 5, the threshold for upsets due to drain strikes increases markedly once the thinning process reaches the epi material (about 2 μm for CMOS6). This is not unexpected, since a rule of thumb is that the charge collection depth is about the epi thickness. This means that for the thinning process to be effective, a significant portion of the epi material needs to be removed. Unfortunately, strikes to the center of the gate begin to dominate the SEU response as the drain strike location

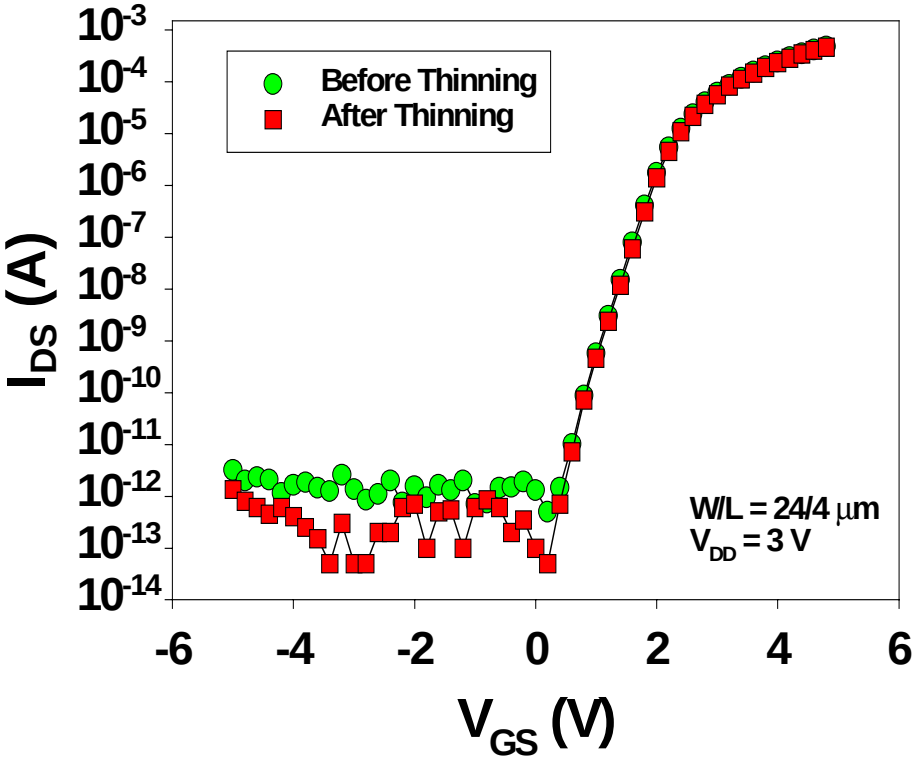

Figure 4. Measured subthreshold current-voltage characteristics for a 24x4 μm n-channel transistors fabricated in a 2μm NMOS process before and after thinning to a substrate thickness of about 5 μm.

becomes less sensitive. This also should not be unexpected, because as the substrate is thinned the device starts to look like a body-tied SOI transistor, and typical body-tied SOI structures exhibit gate-strike limited upset thresholds of about 20-30 MeV-cm^2/mg.

Future Directions

We plan to continue simulations of the SEU response of thinned substrate devices by scaling the simulated devices to gate lengths of 0.25 μm and reduced power supply voltages. We see no reason to believe that the characteristics will be fundamentally different than those shown in Figs. 3 & 5, but we will extend the simulations to the deep submicron level, which is of most interest.

Other Activity

While it is not expected that the total dose response of ICs will be changed by the wafer thinning process, SNL is currently in the process of packaging LLNL devices for total dose testing. It is expected that the exercise of packaging the devices will also help reveal any sources of incompatible processes or steps of the transfer process. LLNL is also developing a 6" silicon wafer transfer process. Equipment is being upgraded to handle 6" wafers. Other efforts are focusing on ensuring that the bulk silicon removal will stop within 1-2 μm from the circuit backside. Both LLNL and Sandia have compatible GCA 4500 series lithography tools. A GCA mask was designed and purchased to permit exposure of the bond pad areas on the reverse side of the Sandia wafers following thinning. This will allow Sandia to cut and package the 256-Kbit SRAMS for SEU testing using the procedure performed for the LLNL devices fabricated on 4" wafers.

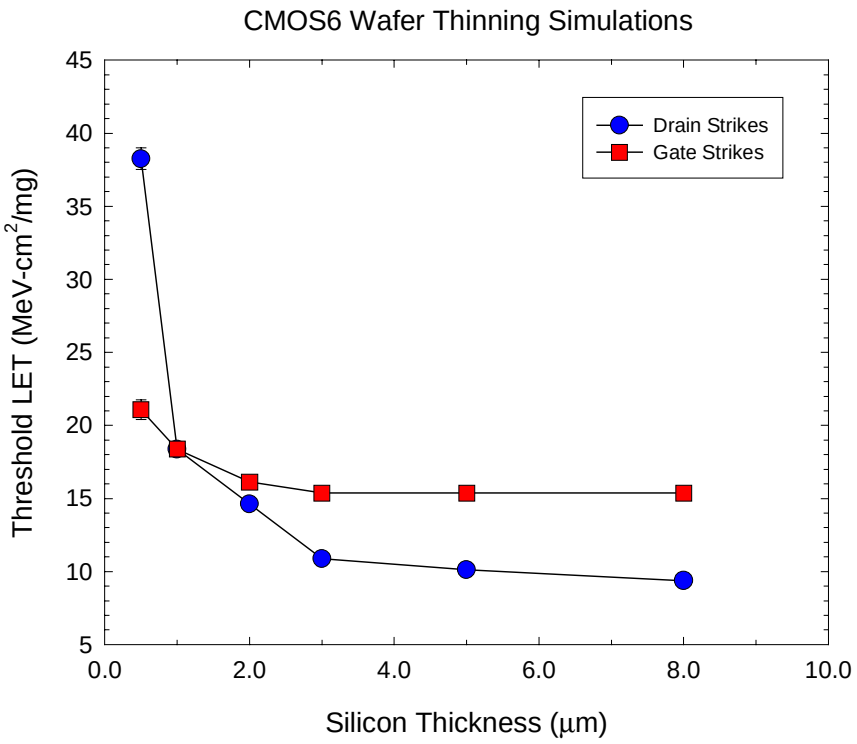

Figure 5. Simulated upset threshold in CMOS6 SRAMs as a function of the substrate thickness. Thresholds are shown for strikes to both the gate and drain of the n-channel transistor biased in an “off” state (the most SEU-sensitive transistor).